WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Wednesday, April 07, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L11	L9.clm.	4
☐	L10	L9.ab.	33
☐	L9	L5 same (time or timing or period)	209
☐	L8	L5.clm.	56
☐	L7	l1 and l5	0
☐	L6	L5.ab.	170
☐	L5	L4 same ((rout$4 or pass$4 or send$4 or transfer$4 or transmit$4) near2 data)	673
☐	L4	L3 same (convert$4 or translat$4)	3597
☐	L3	((read$4 or receiv$4) near2 output near2 data)	28621
☐	L2	L1 same (convert$4 or translat$4)	11
☐	L1	(digital near2 microelectronic near2 circuit)	116

END OF SEARCH HISTORY

First Hit Fwd Refs

Generate Collection Print

L2: Entry 1 of 11 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5936315 A
TITLE: Driving data recording device for motor vehicle mounted directly on or in the drive gear housing shell

Detailed Description Text (7):
A signal generated by the sensor 201 is brought, if necessary, by a signal conditioning stage, in a suitable, advantageously pulse form and is transmitted via a conduit 231 to one of a plurality of interrupt inputs of a control module 202 associated, in accordance with the state of the art, with a microprocessor, microcontroller or any other suitable digital microelectronic circuit. Thereby, the control module 202 updates, e.g., in accordance with instructions of a predetermined program, with each positive increased leading edge of such pulse signal, those distance-dependent data and stored information which later serves for the reconstruction of the distance-time curve or the speed-time curve. The control module 202 can be formed as a distributing center of the trip recorder as it coordinates the entire management and processing of data. The signal generated by the sensor 201 is simultaneously transmitted to a driver stage 210 which amplifies or converts the signal so that it has, when being transmitted via the signal conductor 6, a sufficiently high signal/noise ratio, and which takes care that accidental or intentional external voltage accompanying the signal in the signal conductor 6, normally has no negative effect on data recordings.

L2: Entry 4 of 11 File: USPT Jun 18, 1996

DOCUMENT-IDENTIFIER: US 5528217 A
TITLE: Collision avoidance system for vehicles using digital logic circuitry and retro-fitting techniques

Brief Summary Text (9):
The present invention provides the unique advantage of an electrical wiring system that may be adapted to the traditional wiring system utilizing low power voltage to drive microelectronic digital logic circuitry powered by the vehicle's existing battery system. More specifically, microelectronic digital logic circuits of the present invention uses high frequency acoustical waves transmitted and received returned echo signals to develop time-to-distance ranging signals of remote exterior objects that are processed and converted into preselected incremental and exact distances from the vehicle's exterior perimeter to thereby provide continuous monitoring for collision avoidance. Such distances are presented as warnings as a three digit numerical display, multi-distance discrete color display and audio warnings so as to avoid collisions with exterior objects in close proximity thereto. The three digit numerical display is generated by use of digital logic circuitry having time-to-distance conversion circuits which in combination with digital binary counter circuits therein, generate the numerical display. While the multi-color display of distances to objects and the audio warning alarms are generated by means of digital logic circuitry having at least three voltage comparator circuits for generating the logic signals required to actuate the color display and audio warning alarms.

Brief Summary Text (12):
Yet another object of the invention is the provision of a unique microelectronic digital logic circuit system for generating ongoing time-to-distance parameters from transmit and received echo signals from exterior bodies that may cause collision incidents which are converted into priority encoded signals representing at least three discrete distances within a preselected range of distances for continuous display thereof and at least two discrete distances within a range of distances for audio warnings and utilizing such signals to generate corresponding three digit numerical displays as an aid to verification of such distances.

L2: Entry 5 of 11 File: USPT May 18, 1993

DOCUMENT-IDENTIFIER: US 5212484 A
TITLE: Digital to analog converter system employing plural digital to analog converters which is insensitive to resistance variations

Brief Summary Text (8):
Several basic types of digital to analog converter circuits are known, as is generally described in, for example, J. Millman, Microelectronics: Digital and Analog Circuits And Systems (New York: McGraw-Hill Book Company, 1979) at pp. 606-609. Generally, digital to analog converter circuits include an operational amplifier that amplifies a voltage at an input terminal, which voltage it receives from a resistor network. The resistor network is generally connected to two distinct reference voltages, one of them typically a ground voltage and receives a number of signals, each representative of the condition of bits of the digital word being "converted." The conditions of the diverse bits of the digital word effectively control selected ones of the resistors to connect resistors to one of the two reference voltages. If the resistance values of the resistors forming the resistor network could be made perfect, which could be quite expensive, changes in the numerical value of the digital word controlling the resistor network would result in a proportional change in the voltage applied to the input terminal of the operational amplifier and thus a proportional change in its output voltage level. However, manufacturing variations of the resistors used in implementing an actual digital to analog converter circuit of reasonable cost result in some tolerance in their actual resistor values, in which case changes in voltage levels generated by a digital to analog converter do not necessarily change in direct proportion to changes in the values of the digital word applied thereto. Indeed, the variations in resistance values may, in an actual circuit, be sufficiently large that changes in voltage levels may not be monotonic with changes from one value of the digital word to the next higher or lower value.

Detailed Description Text (4):
The digital to analog converters 11i are preferably similar to each other, and may comprise any conventional digital to analog converter circuit, circuits for which are described in the aforementioned J. Millman, Microelectronics: Digital and Analog Circuits And Systems (New York: McGraw-Hill Book Company, 1979) at pp. 606-609. A circuit for a new digital to analog circuit suitable for use in connection with the digital to analog conversion system 10, which forms a further aspect of the invention, is shown as digital to analog converter 11A in the Figure. Digital to analog converter 11A includes a register 20, which receives and stores the DIG WRD A digital word "A" signals from the control circuit 12, an operational amplifier circuit 21, and a resistor ladder circuit 22.

L2: Entry 6 of 11 File: USPT Aug 18, 1992

DOCUMENT-IDENTIFIER: US 5140248 A
** See image for Certificate of Correction **
TITLE: Open loop motor control with both voltage and current regulation

Detailed Description Text (24):
The I*.sub.qe signal is current-limited by executing the current limit portion 30d of the program, and is then applied to a DC-to-AC portion 30e of the program which converts the I*.sub.qe signal to a pair of AC command signals I*.sub.q and I*.sub.d having a phase difference of 90.degree.. The CPU 30a generates digital values for .theta..sub.e which are applied as a second input to the DC-to-AC portion 30e of the program. The resulting command signals I*.sub.qs and I*.sub.ds are then applied to a pair of MDAC circuits 25 and multiplied by V.sub.REF to convert the digital outputs of the microelectronic processing circuit 30 to analog signals for input to the synchronous current regulator 16.

L2: Entry 7 of 11 File: USPT Sep 18, 1990

DOCUMENT-IDENTIFIER: US 4958117 A
** See image for Certificate of Correction **
TITLE: Frequency control based on sensing voltage fed to an induction motor

Detailed Description Text (29):
The current commands I*.sub.qs and I*.sub.ds are applied to a pair of MDAC circuits 25 and multiplied by V.sub.REF to convert the digital outputs of the microelectronic processing circuit 30 to analog signals for input to the current regulator 16.

First Hit Fwd Refs

Generate Collection Print

L11: Entry 1 of 4 File: USPT Aug 6, 2002

DOCUMENT-IDENTIFIER: US 6430225 B1
TITLE: Apparatus and method for digital data transmission

CLAIMS:

37. A data transmission method for carrying out transmission/reception of data and control code, the data transmission method comprising: a transmit data converting processing step of converting the data to be transmitted from n bit code to m bit code and passing the resulting m bit code to an input/output port; a receive data converting processing step of converting the data received from the input/output port from m bit code to n bit code; a transmit control signal converting processing step of converting a transmit control signal for arbitrating use of a transmission path connected to the input/output port into an arbitration control code comprising m bit code, except for m bit code allocated to the data to be transmitted, wherein the transmit control signal converting processing step converts an idle signal transmitted for a time period during which no data is transmitted into m bit code, in which bit values "1" are continuous; and a receive control signal converting processing step of converting a received control code of m bits received from the input/output port into a received control signal.

42. A data transmission apparatus adapted for carrying out transmission/reception of data and control code, comprising: an input/output port; a converting processing block: (a) for converting the data to be transmitted from said input/output port from n bit code to m bit code, wherein m>n, and passing the resulting m bit code to the input/output port, (b) for converting the data received from the input/output port from m bit code to n bit code, (c) for converting an arbitration signal arbitrating use of a transmission path connected to the input/output port into an m bit arbitration control code, and (d) for converting an m bit received arbitration control code received from the input/output port into a received arbitration signal; wherein the converting processing block converts an idle signal transmitted for a time period during which no data is transmitted into m bit code in which all m bits are "1".

L11: Entry 2 of 4 File: USPT Jul 16, 2002

DOCUMENT-IDENTIFIER: US 6421291 B1
TITLE: Semiconductor memory device having high data input/output frequency and capable of efficiently testing circuit associated with data input/output

CLAIMS:

1. A semiconductor memory device internally converting serial data supplied from and to any external unit into parallel data and executing reading and writing operations thereof, comprising: a memory cell array having a plurality of memory cells arranged in rows and columns; a data terminal for input and output of N data (N: natural number) transmitted in time series manner; and a data input/output circuit for reading and writing said N data from and into said memory cell array; said data input/output circuit including: N write data lines and N read data lines for transmitting said N data in parallel; a first data conversion circuit which converts N serial data supplied from said data terminal into N parallel data to transmit the parallel data to said N write data lines respectively; a second data conversion circuit which converts N parallel data transmitted by said N read data lines into N serial output data to be output from said data terminal; a read and write circuit for supplying and receiving said N data between said N write data lines and said memory cell array and between said N read data lines and said memory cell array; and an input/output test circuit which transfers data transmitted by said N write data lines respectively to said N read data lines in an input/output test operation.

L11: Entry 3 of 4 File: USPT Jan 4, 1994

DOCUMENT-IDENTIFIER: US 5276727 A
** See image for Certificate of Correction **
TITLE: Remote maintenance method and device thereof in private branch exchange system

CLAIMS:

4. A private branch exchange system having a remote maintenance capability, said system comprising:

controlling means for controlling in overall operation of said private branch exchange system, for receiving inquiries from a remote maintenance center through a public switch telephone network, for generating replies to said inquiries to be provided to said remote maintenance center through said public switch telephone network, and for controlling maintenance functions of said private branch exchange system in response to results generated by said remote maintenance center by diagnosing said private branch exchange system according to analysis of said replies;

switching means for establishing a data communication path between said remote maintenance center and said controlling means through said public switch telephone network;

input/output means for receiving said replies as output parallel bus data from said controlling means, for converting said output parallel bus data to output serial local bus data, for receiving said inquiries and said results as input series local bus data, and for converting input serial local data to input parallel bus data to be provided to said controlling means;

means for receiving and modulating said output serial local bus data to generate output analog data signals, and for receiving and demodulating input analog data signals to generate said input serial local bus data; and

codec means for receiving and converting said output analog data signals to output digital data signals and transmitting said output digital data signals to said switching means in a selected time slot, and for receiving input digital data signals of a given time slot and for converting said input digital data signals to said input analog data signals received by said modulating and demodulating means.

First Hit Fwd Refs
End of Result Set

Generate Collection Print

L11: Entry 4 of 4 File: USPT Mar 27, 1973

DOCUMENT-IDENTIFIER: US 3722434 A
TITLE: DIGITAL PATTERN CONTROL APPARATUS FOR TEXTILE MACHINERY

CLAIMS:

5. In combination in apparatus for providing a digital record of pattern information characterizing a pattern to be formed in textile goods by the selective actuation of plural pattern forming stations during a single textile forming stitch, scanning means for scanning patterns in the direction of the desired textile stitch and for providing an output characterizing said pattern along the scanning direction, digital quantizing means for quantizing the output of said scanning means, strobe means operative in synchronization with said scanning means for sampling the output of said quantizing means at a plurality of spaced locations along said scanning direction, series-to-parallel converter means for converting subsets of said sampled output digits from said scanning and quantizing means into parallel form, scan line timing means associated with said strobe means for providing a signal at a predetermined point during the relative travel of said scanning means along said scan direction, stitch signaling means connected to said scan line timing means for generating a control signal at a predetermined point during data processing for each stitch, data storing means for storing the output of said series-to-parallel converter means and said control signal supplied by said stitch signaling means, a tufting machine controller including data reading means for reading the data recorded by said data storing means, a present stitch register, a next stitch register, timing means adapted to be driven by the tufting machine for supplying a signal indicative of the completion of a stitch by the tufting machine, control means responsive to said end of stitch signal for transferring data from said next stitch register to said present stitch register and for activating said data reading means for entering information descriptive of the next stitch into said next stitch register, said next stitch register controlling means including means for counting said data subsets read by said data reading means, means for decoding the output of said counter means, said next stitch register being formed of a plurality of register modules, additional decoding means selectively connected to said subset counter decoding means for sequentially enabling said next stitch register modules, and means for supplying data from said reading means in parallel to said next stitch register modules.

First Hit Fwd Refs

Generate Collection Print

L8: Entry 1 of 56 File: USPT Apr 6, 2004

DOCUMENT-IDENTIFIER: US 6718122 B1
TITLE: Image processing apparatus

CLAIMS:

10. An image processing apparatus for processing digital image data using a first memory and a second memory, comprising: a first data bus, adapted to transfer digital image data of a first format according to an order of scanning on an image frame, said first memory being connected to said first data bus and being adapted to store the digital image data of the first format, said first memory inhibiting digital image data of a second format for recording of the digital image data on a recording medium from being written into and read from said first memory through said first data bus; an input device, connected to said first data bus, adapted to input digital image data of the first format and write the input image data of the first format into said first memory through said first data bus; a second data bus, separate from said first data bus, adapted to transfer digital image data of a second format, said second memory being connected to said second data bus and being adapted to store the digital image data of the second format, said second memory inhibiting the digital image data of the first format from being written into and read from said second memory through said second data bus; a data transmitter, connected to said first data bus and said second data bus, adapted to read the digital image data of the first format from said first memory through said first data bus, convert the first format of the digital image data read out from said first memory to provide converted digital image data of the second format, and transmit the converted digital image data of the second format to said second memory through said second data bus, said data transmitter also being adapted to read the digital image data of the second format from said second memory through said second data bus, convert the second format of the digital image data read out from said second memory to provide converted digital image data of the first format, and transmit the converted digital image data of the first format to said first memory through said first data bus; and an output device, connected to said second data bus, adapted to read the digital image data of the second format from said second memory through said second data bus and to output the read digital image data of the second format so that the digital image data of the second format are recorded on a recording medium.

18. An image processing apparatus comprising: a first data bus, adapted to transfer digital image data of a first format according to an order of scanning on an image frame; a first memory, connected to said first data bus, adapted to store the digital image data of the first format, said first memory inhibiting digital image data of a second format for recording of the digital image data on a recording medium from being written into and read from said first memory through said first data bus; a second data bus, separate from said first data bus, adapted to transfer digital image data of the second format; a second memory, connected to said second data bus, adapted to store the digital image data of the second format, said second memory inhibiting the digital image data of the first format from being written into and read from said second memory through said second data bus; a data reproducer, connected to said second data bus, adapted to reproduce digital image data of the second format from a recording medium and to write the reproduced digital image of the second format into said second memory through said second data

bus; a data transmitter, connected to said first data bus and said second data bus, adapted to read the digital image data of the second format from said second memory through said second data bus, convert the second format of the digital image data read out from said second memory to provide converted digital image data of the first format, and transmit the converted digital image data of the first format to said first memory through said first data bus, said data transmitter also being adapted to read the digital image data of the first format from said first memory through said first data bus, convert the first format of the digital image data read out from said first memory to provide converted digital image data of the second format, and transmit the converted digital image data of the second format to said second memory through said second data bus; and an output device, connected to said first data bus, adapted to read the digital image data of the first format from said first memory through said first data bus and output the read digital image data of the first format to outside of said apparatus.

L8: Entry 2 of 56 File: USPT Mar 23, 2004

DOCUMENT-IDENTIFIER: US 6711160 B2
TITLE: Packet network telephone interface system for POTS

CLAIMS:

1. A packet network telephone interface system for enabling communications with plain old telephone sets over a plurality of telecommunications networks, said system comprising: telephone input/output units for receiving signals from and transmitting signals to a plain old telephone set and a public switched telephone network; a network connection input/output unit for receiving data packets directly from and transmitting data packets directly to a data packet based network having a defined network protocol; a processing subsystem including a network interface card, located in series between the network connection unit and the telephone input/output units, for converting signals from the plain old telephone set into data packets in accordance with said defined network protocol for transmission over the data packet based network, and for converting data packets from the data packets based network into signals suitable for transmission to the plain old telephone set, the processing subsystem including; at least one dual coder/decoder connected to the input/output units for converting analog signals into digital signals, and for converting digital signals into analog signals; switching means to determine whether signals from the plain old telephone are transmitted to the telephone network, or to the network interface card for conversion into data packets for transmission to the data packet based network.